WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device, comprising:

forming a gate oxide over a substrate and a gate electrode over the gate oxide;

implanting impurities into the substrate using the gate electrode as an implant mask to form a lightly-doped region in the substrate;

depositing second spacer material adjacent the gate electrode;

forming a first spacer on the second spacer material;

implanting impurities into the substrate and through a portion of the lightly-doped region using the first spacer as an implant mask to form a first junction region in the substrate;

removing the first spacer;

etching the second spacer material to form a second spacer adjacent the gate electrode; and

implanting impurities into the substrate using the second spacer as an implant mask to form a second junction region in the substrate.

2. The method of Claim 1, further including depositing additional second spacer material on the initially deposited second spacer material prior to etching the second spacer material.

3. The method of Claim 1, wherein said first junction region is a deep junction region and said second junction region is a source/drain region.

4. The method of Claim 1, wherein said first spacer comprises an oxide, and said second spacer material comprises a nitride.

5. The method of Claim 1, wherein the second spacer has a width less than a width of the first spacer.

6. The method of Claim 3, further including forming a silicide over the source/drain region.

7. The method of Claim 1, wherein the substrate is a silicon-on-insulator substrate.

8. The method of Claim 1, wherein the lightly-doped region has a dopant concentration in the range of about $1 \times 10^{18}cm^{-3}$ to about $1 \times 10^{20}cm^{-3}$.

9. The method of Claim 1, wherein the first junction region has a dopant concentration in the range of about $1 \times 10^{17}cm^{-3}$ to about $1 \times 10^{20}cm^{-3}$.

10. The method of Claim 1, wherein the second junction region has a dopant concentration in the range of about $1 \times 10^{18}cm^{-3}$ to about $1 \times 10^{21}cm^{-3}$.

11. A method of manufacturing a short channel semiconductor device, comprising:

forming a gate oxide over a substrate and a gate electrode having a gate width of less than 0.13 micron over the gate oxide;

implanting impurities into select regions of the substrate using the gate electrode as an implant mask to form a lightly-doped region in the substrate having a channel region extending therebetween beneath the gate oxide, the channel region having a channel length of less than 0.13 micron;

depositing a bottom layer over the gate electrode and the substrate, and an upper layer over the bottom layer;

removing portions of the upper layer to form a first spacer adjacent the gate electrode;

implanting impurities through a portion of the lightly doped region using the first spacer as an implant mask to form a first junction region in the substrate;

removing the first spacer;

removing portions of the bottom layer to form a second spacer adjacent the gate electrode; and

implanting impurities through a portion of the lightly doped region and into the substrate using the second spacer as an implant mask to form a second junction region in the substrate.

12. The method of Claim 11, further including depositing additional bottom layer material on the initially deposited bottom layer prior to removing portions of the bottom layer to form the second spacer.

13. The method of Claim 11, wherein said first junction region is a deep junction region and said second junction region is a source/drain region.

14. The method of Claim 11, wherein depositing an upper layer comprises depositing an upper layer comprising an oxide, and wherein depositing a bottom layer comprises depositing a bottom layer comprising a nitride.

15. The method of Claim 11, wherein removing portions of the bottom layer to form a second spacer further comprises removing portions of the bottom layer to form a second spacer having a width less than a width of the first spacer.

16. The method of Claim 11, further including forming a silicide over the second junction region.

17. The method of Claim 11, wherein the substrate is a silicon-on-insulator substrate.

18. The method of Claim 11, further including:

forming a dielectric over the gate electrode and the second junction region;

forming a contact opening through said dielectric; and

forming an interconnect in said contact opening, the interconnect being electrically coupled to said second junction region.

19. The method of Claim 11, wherein removing the first spacer comprises performing an etch step using hot H_3PO_4 acid.

20. The method of Claim 11 further comprising forming a liner layer on the gate electrode and the substrate prior to depositing the bottom layer.

21. A semiconductor device comprising:

a gate structure formed over a semiconductor region;

a lightly doped source/drain region formed in the semiconductor region to a first depth, the lightly doped source/drain region substantially aligned with a sidewall of the gate structure;

a sidewall spacer formed along a sidewall of the gate structure;

a heavily doped source/drain region formed in the semiconductor region to a second depth deeper than the first depth, the heavily doped source/drain region substantially aligned with an outer edge of the sidewall spacer; and

a deep source/drain region formed in the semiconductor region to a third depth deeper than the second depth, the deep source/drain region spaced a lateral distance from the outer edge of the sidewall spacer.

22. The device of claim 21 and further comprising:

a second sidewall spacer formed along a second sidewall of the gate structure;

a second lightly doped source/drain region formed in the semiconductor region to the first depth, the second lightly doped source/drain region substantially aligned with a second sidewall of the gate structure;

a second heavily doped source/drain region formed in the semiconductor region to the second depth, the second heavily doped source/drain region substantially aligned with an outer edge of the second sidewall spacer; and

a second deep source/drain region formed in the semiconductor region to the third depth, the second deep source/drain region spaced a lateral distance from the outer edge of the second sidewall spacer.

23. The device of claim 21 wherein the lightly doped source/drain region, the heavily doped source/drain region, and the deep source/drain region are formed from impurities of the same conductivity type.

24. The device of claim 23 wherein the lightly doped source/drain region, the heavily doped source/drain region, and the deep source/drain region are formed from impurities of the same material.

25. The device of claim 21, further comprising a silicide region formed at the surface of the semiconductor region adjacent the outer edge of the sidewall spacer.